MOSFET - N-Channel Shielded Gate PowerTrench®

150 V, 7.3 mΩ, 101 A

NTP7D3N15MC

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 7.3 mΩ at V_{GS} = 10 V, I_D = 62 A
- 50% Lower Qrr than other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	150	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	101	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	166	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	12.1	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			P_D	2.4	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs		I_{DM}	574	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy (I_L = 20 A_{pk}, L = 3 mH)			E_{AS}	600	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

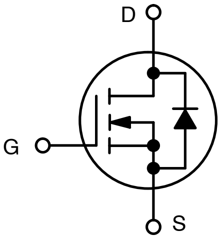
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

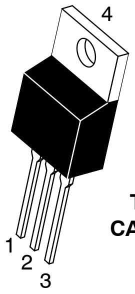
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	7.3 mΩ @ 10 V	101 A

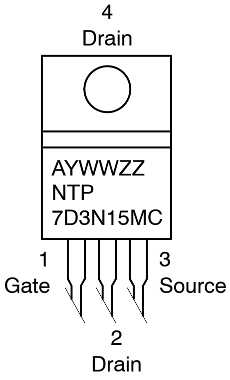


N−CHANNEL MOSFET



TO−220 CASE 221A

MARKING DIAGRAM



NTP7D3N15MC = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTP7D3N15MC	TO−220 (Pb−Free)	800 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	62.5	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	150			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 µA, ref to 25°C		71		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V; T_J = 25°C			1.0	µA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 342 µA	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 342 µA, ref to 25°C		−7.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 62 A		6.2	7.3	mΩ
		V_{GS} = 8 V, I_D = 31 A		6.6	8.4	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 62 A		119		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 75 V		4250		pF
Output Capacitance	C_{OSS}			1250		
Reverse Transfer Capacitance	C_{RSS}			15		
Gate−Resistance	R_G			0.8	1.6	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 75 V; I_D = 62 A		53		nC
Threshold Gate Charge	$Q_{G(TH)}$			14		
Gate−to−Source Charge	Q_{GS}			23		
Gate−to−Drain Charge	Q_{GD}			8.5		
Plateau Voltage	V_{GP}			5.8		V
Output Charge	Q_{OSS}	V_{DD} = 75 V, V_{GS} = 0 V		133		nC
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 75 V, I_D = 62 A, R_G = 4.7 Ω		27		ns
Rise Time	t_r			8.5		
Turn−Off Delay Time	$t_{d(OFF)}$			33		
Fall Time	t_f			5.8		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 62 A; T_J = 25°C		0.93	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 300 A/µs, I_S = 62 A		55		ns
Reverse Recovery Charge	Q_{RR}			247		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 1000 A/µs, I_S = 62 A		50		ns
Reverse Recovery Charge	Q_{RR}			720		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

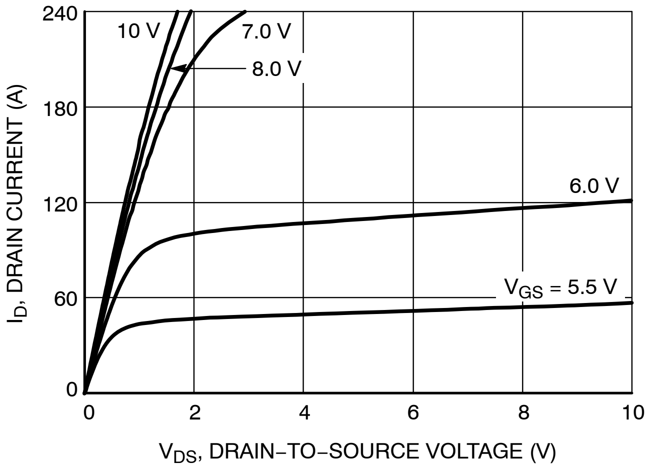


Figure 1. On−Region Characteristics

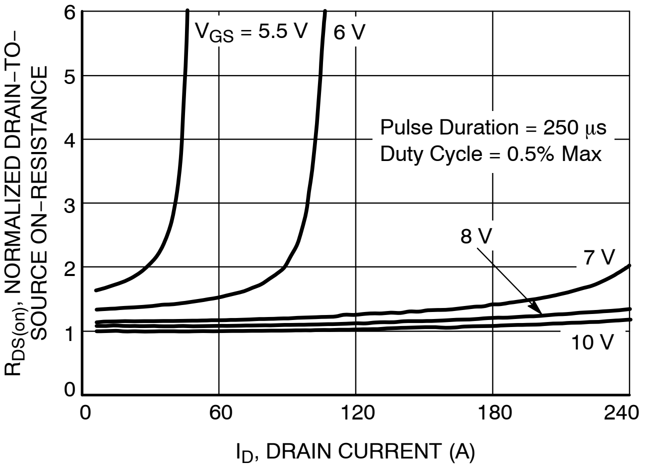


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

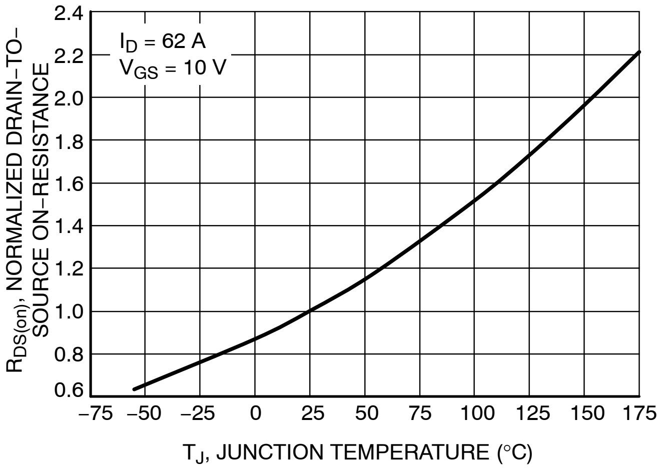


Figure 3. Normalized On−Resistance vs. Junction Temperature

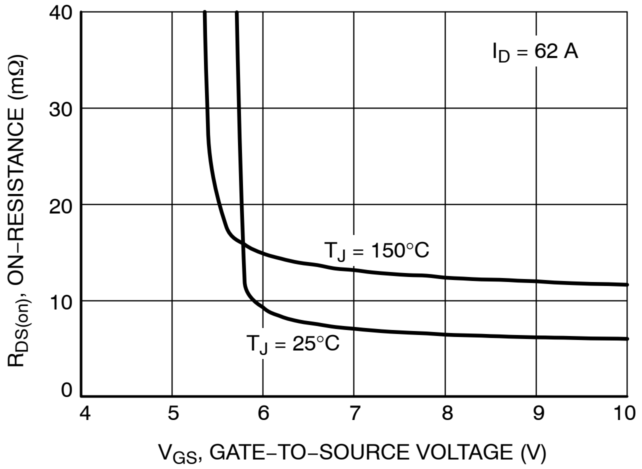


Figure 4. On−Resistance vs. Gate−to−Source Voltage

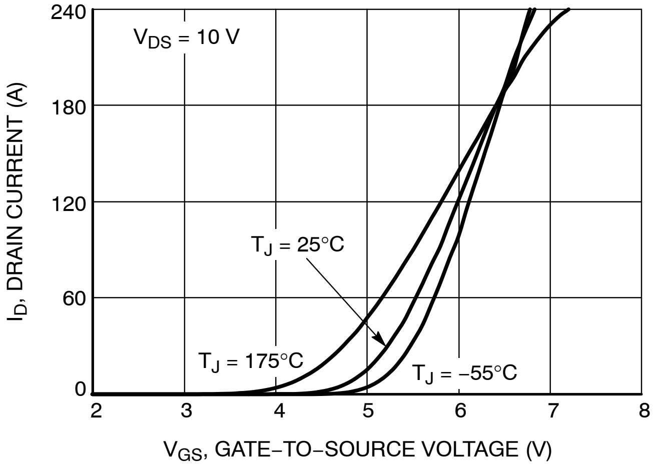


Figure 5. Transfer Characteristics

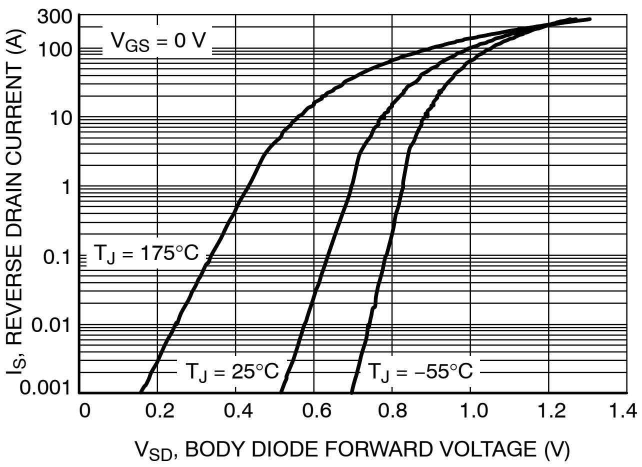


Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

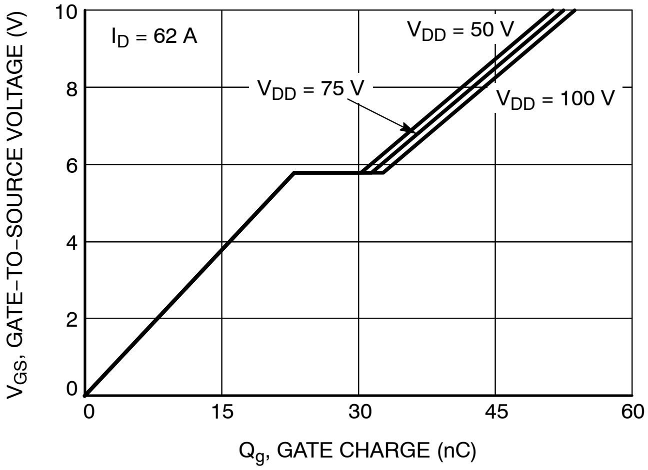


Figure 7. Gate Charge Characteristics

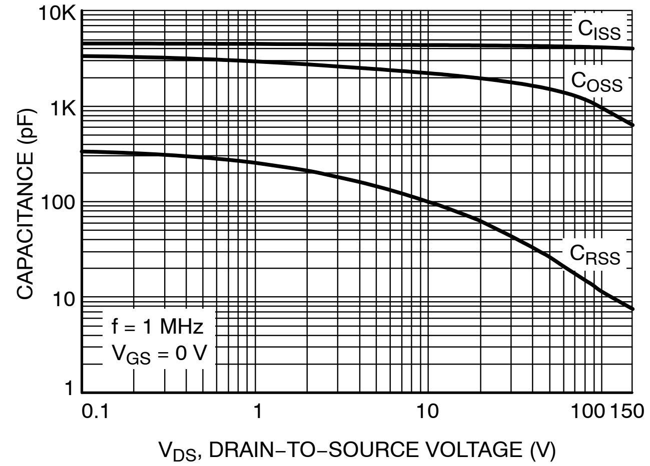


Figure 8. Capacitance vs. Drain−to−Source Voltage

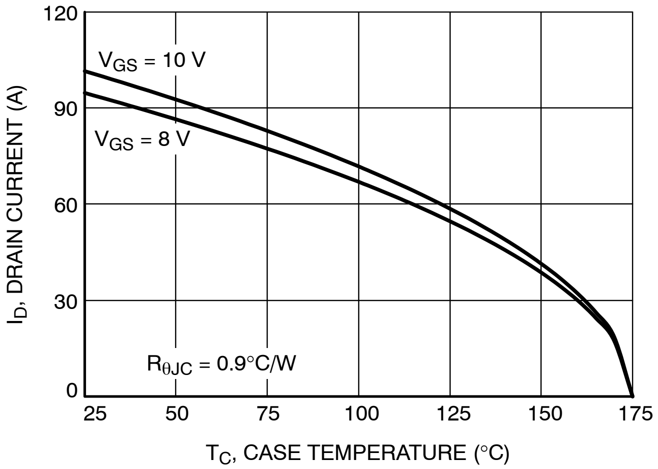


Figure 9. Drain Current vs. Case Temperature

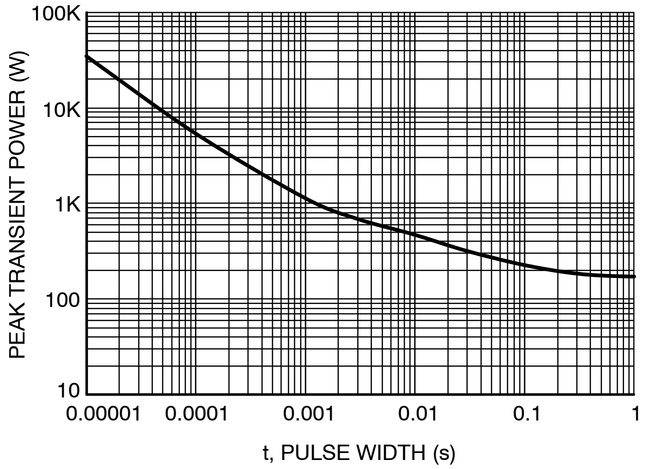


Figure 10. Peak Power

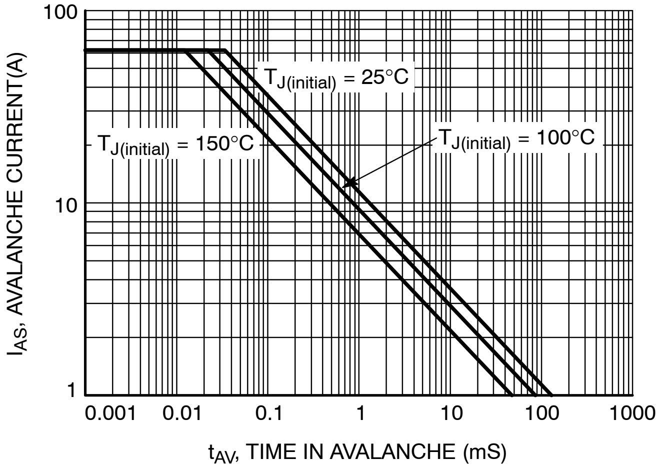


Figure 11. Unclamped Inductive Switching Capability

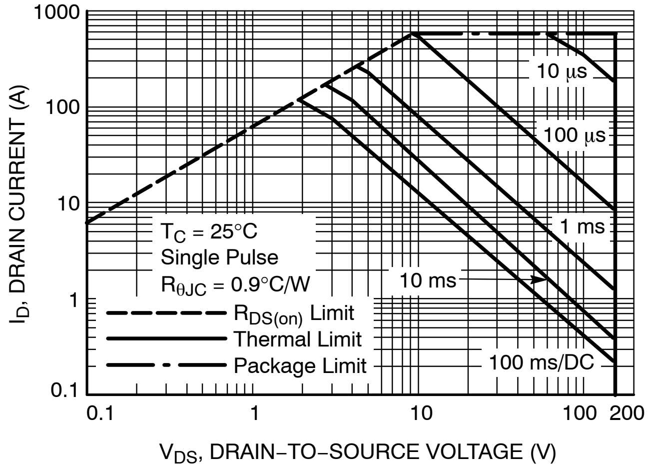
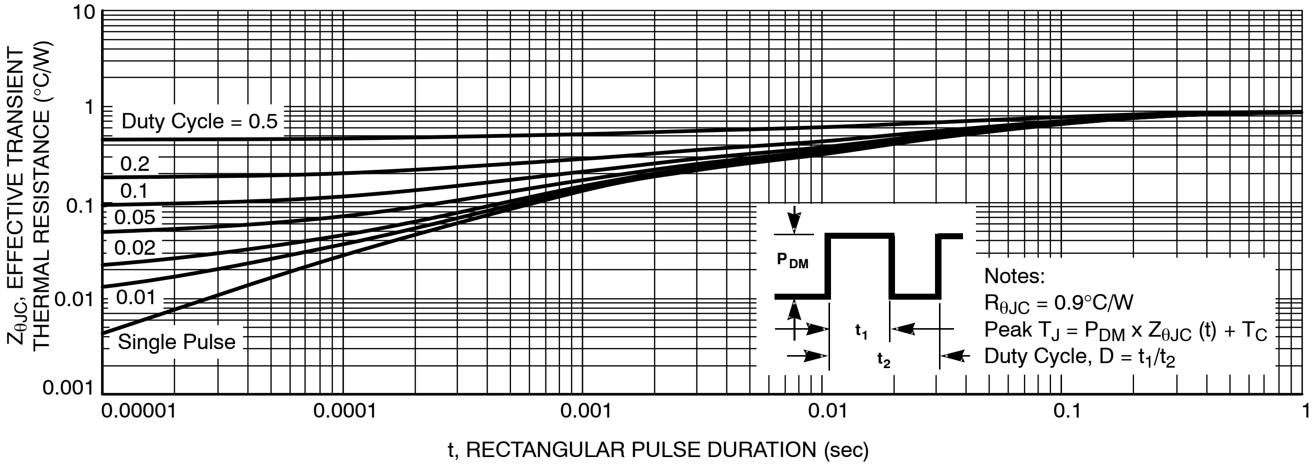


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS



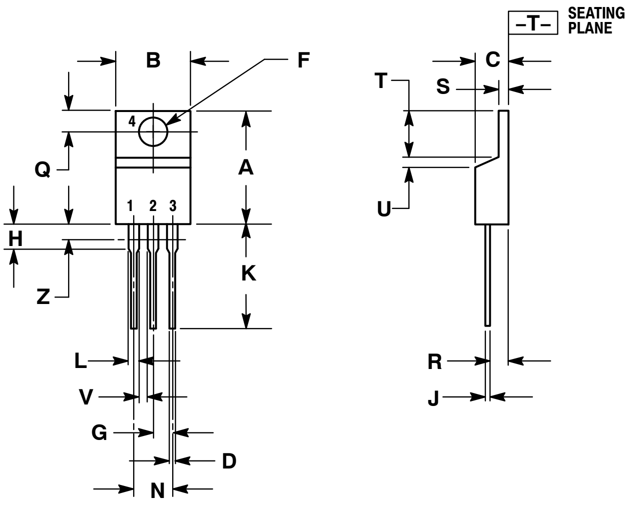
Notes:
$R_{\theta JC}$ = 0.9°C/W
Peak $T_J = P_{DM} \times Z_{\theta JC}(t) + T_C$
Duty Cycle, $D = t_1/t_2$

Figure 13. Transient Thermal Impedance

PACKAGE DIMENSIONS

TO−220

CASE 221A−09
ISSUE AH



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative