

MOSFET – Single N-Channel, SUPERFET® V, FRFET® 600 V, 55 mΩ, 45 A

NVHL055N60S5F

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on) max.} \times Q_{g typ.}$ & $R_{DS(on) max.} \times E_{OSS}$)
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	600	V	
Gate-to-Source Voltage	DC	± 30	V	
	AC ($f > 1 \text{ Hz}$)	± 30	V	
Continuous Drain Current	$T_C = 25^\circ\text{C}$	45	A	
	$T_C = 100^\circ\text{C}$	28	A	
Power Dissipation	$T_C = 25^\circ\text{C}$	275	W	
Pulsed Drain Current	$T_C = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	159	A
Pulsed Source Current (Body Diode)		I_{SM}	159	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	45	A	
Single Pulse Avalanche Energy	($I_L = 7 \text{ A}$, $R_G = 25 \Omega$)	E_{AS}	417	mJ
Avalanche Current	I_{AS}	7	A	
Repetitive Avalanche Energy (Note 1)	E_{AR}	2.78	mJ	
MOSFET dv/dt	dvdt	120	V/ns	
Peak Diode Recovery dv/dt (Note 2)		70		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

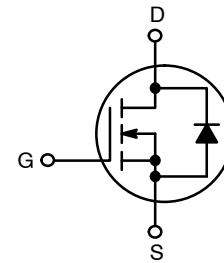
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{SD} \leq 22.5 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq 400 \text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL RESISTANCE

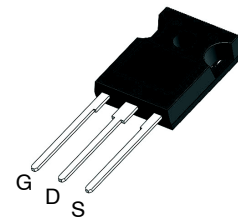
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Notes 3, 4)	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Notes 3, 4)	$R_{\theta JA}$	40	

3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
4. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).

V_{DSS}	$R_{DS(ON) MAX}$	$I_D MAX$
600 V	55 mΩ @ 10 V	45 A

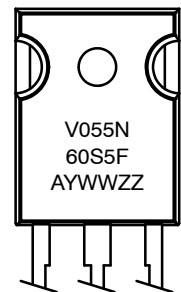


POWER MOSFET



TO-247-3LD
CASE 340CX

MARKING DIAGRAM



V055N60S5F = Specific Device Code
A = Assembly Location
YWW = Data Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
NVHL055N60S5F	TO-247-3LD (Pb-Free)	30 Units / Tube

NVHL055N60S5F

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/\Delta T_J$	$I_D = 10\text{ mA}$, Referenced to 25°C		581		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^\circ\text{C}$			10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}, T_J = 25^\circ\text{C}$		44	55	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 5.2\text{ mA}, T_J = 25^\circ\text{C}$	3.2	4.12	4.8	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(th)}/\Delta T_J$	$V_{GS} = V_{DS}, I_D = 5.2\text{ mA}$		-6.61		mV/ $^\circ\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 22.5\text{ A}$		44.8		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ KHz}$		4603		pF
Output Capacitance	C_{OSS}			72.9		
Energy Related Output Capacitance	$C_{OSS(er)}$	$V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$		125		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, V_{GS} = 10\text{ V}$		85.2		nC
Gate-to-Source Charge	Q_{GS}			26.2		
Gate-to-Drain Charge	Q_{GD}			24.9		
Gate Resistance	R_G	$f = 1\text{ MHz}$		4.32		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, R_G = 4.7\text{ }\Omega$		44		ns
Rise Time	t_r			26.2		
Turn-Off Delay Time	$t_{d(OFF)}$			108		
Fall Time	t_f			2.6		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, T_J = 25^\circ\text{C}$		1.07		V
		$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, T_J = 150^\circ\text{C}$		0.82		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$		128		ns
Reverse Recovery Charge	Q_{RR}			758		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

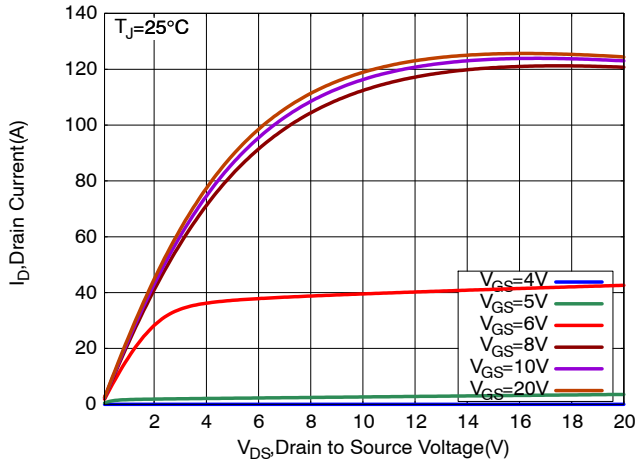


Figure 1. On-Region Characteristics

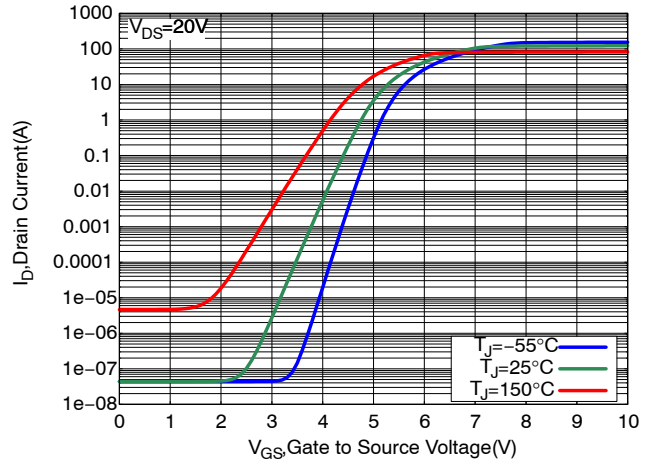


Figure 2. Transfer Characteristics

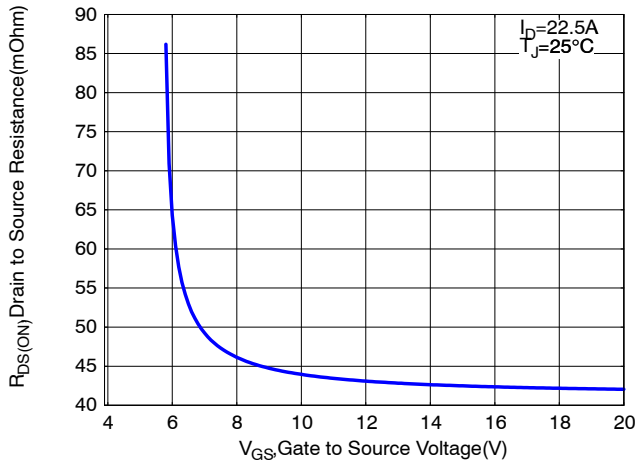


Figure 3. On-Resistance vs. V_{GS}

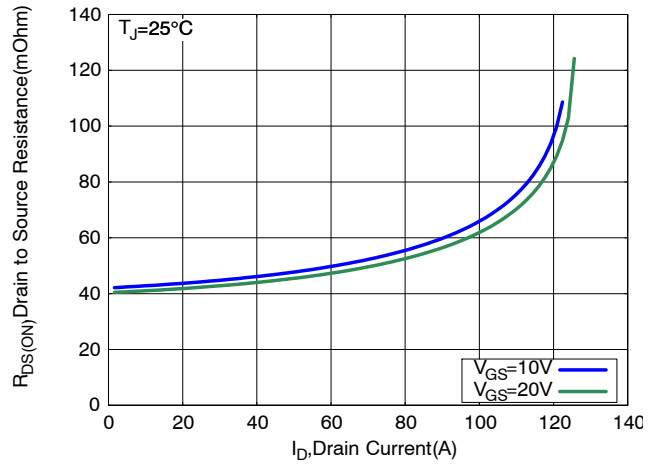


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

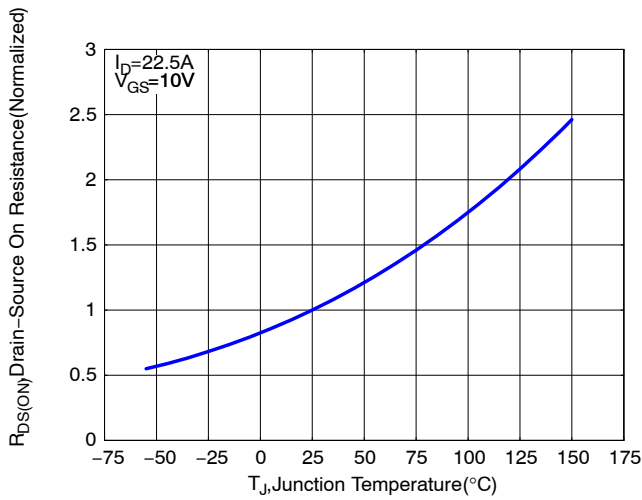


Figure 5. On-Resistance Variation with Temperature

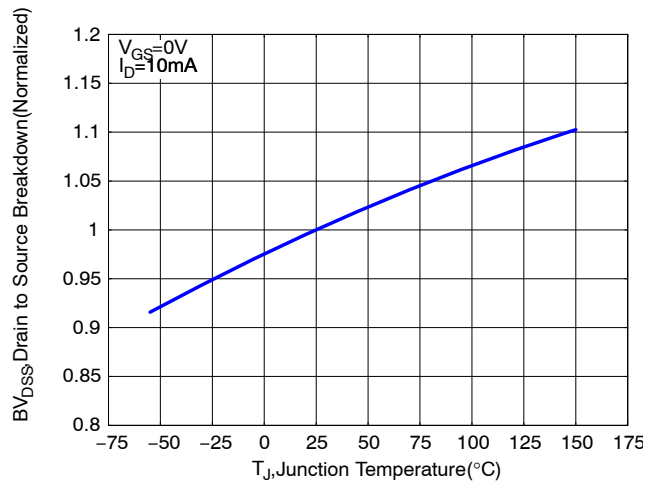


Figure 6. Breakdown Voltage Variation with Temperature

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TYPICAL CHARACTERISTICS

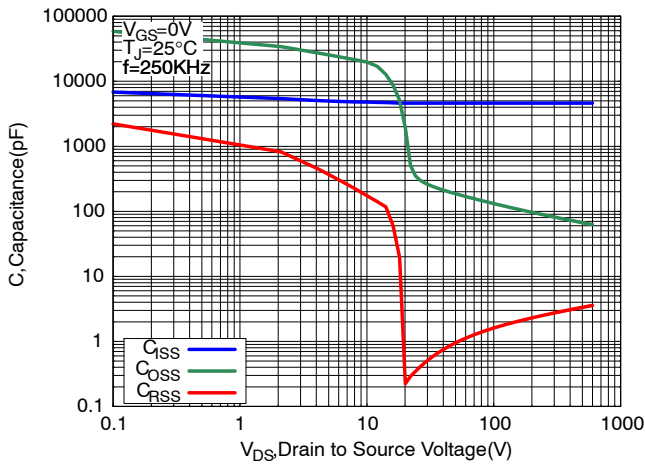


Figure 7. Capacitance Variation

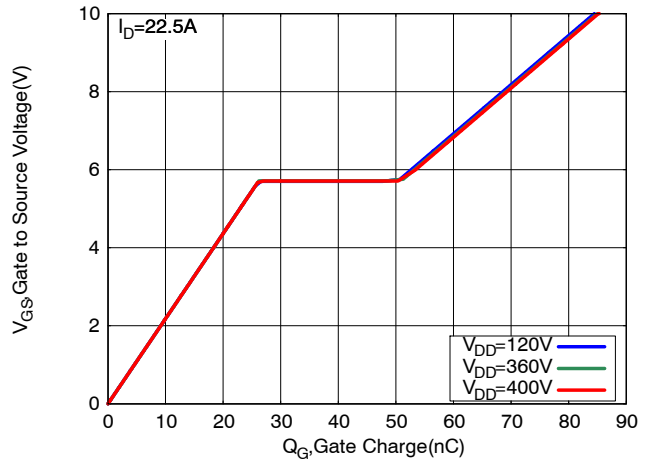


Figure 8. Gate-to-Source Voltage vs. Total Charge

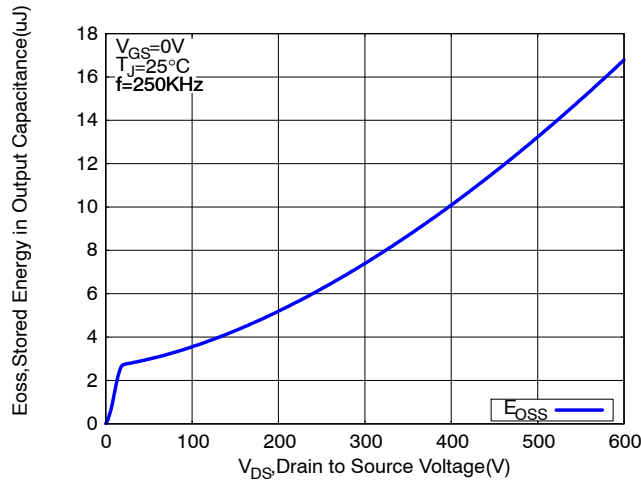


Figure 9. Eoss vs. Drain-to-Source Voltage

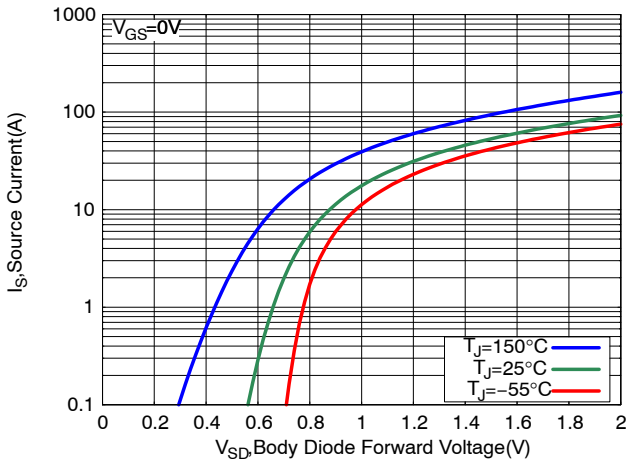


Figure 10. Diode Forward Voltage vs. Current

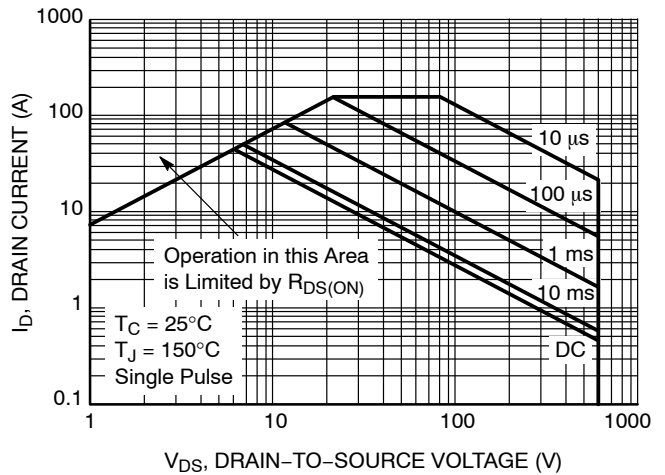


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

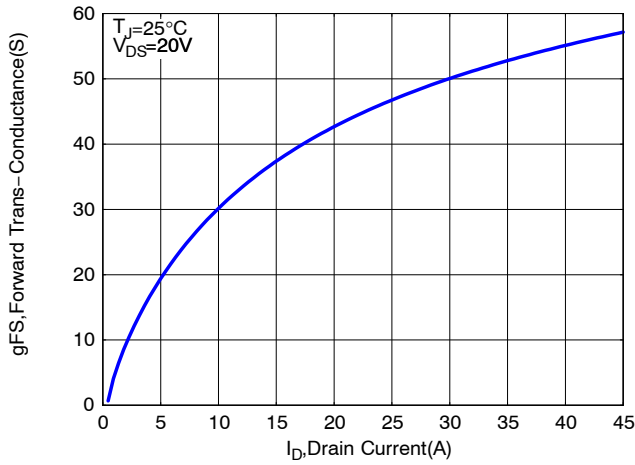


Figure 12. g_{FS} vs. I_D

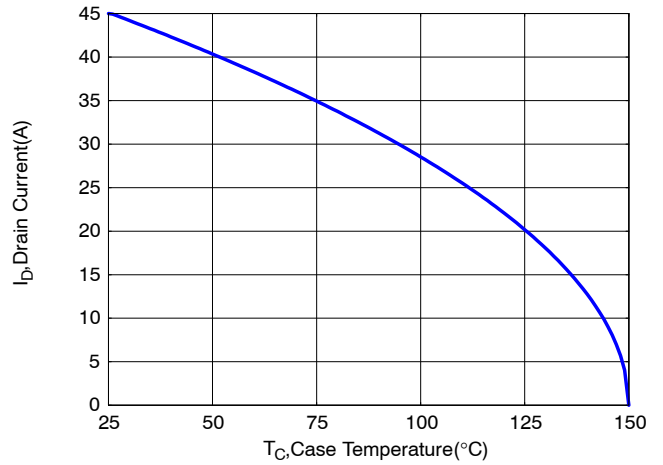


Figure 13. Maximum Current vs. Case Temperature

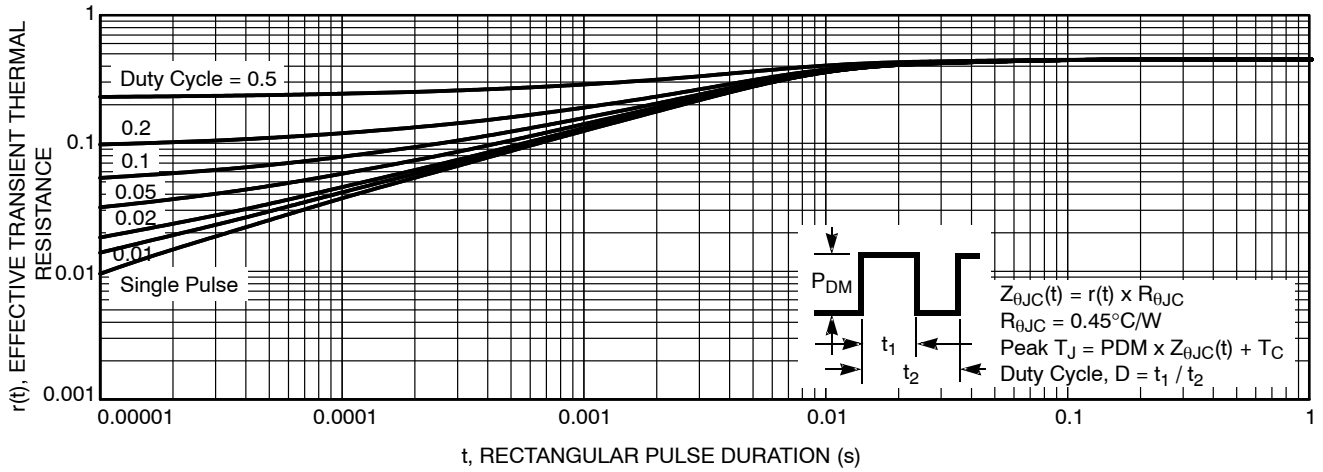


Figure 14. Thermal Response

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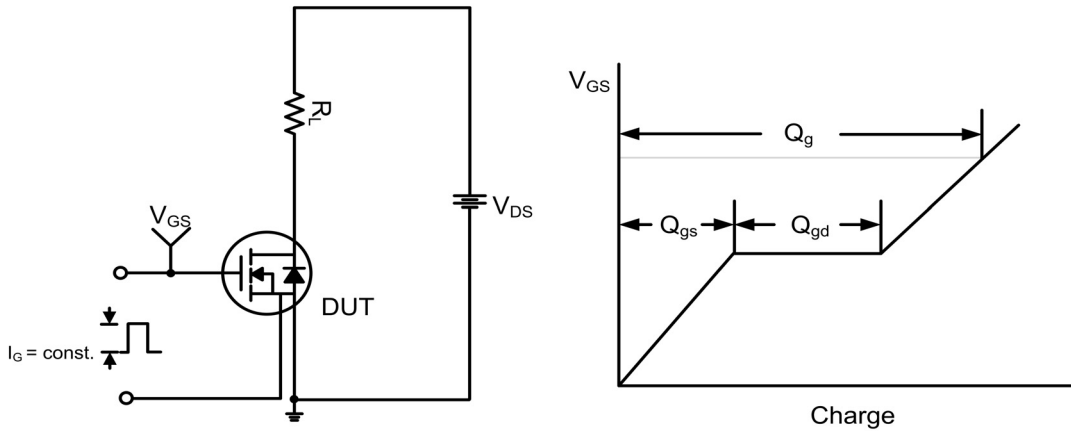


Figure 15. Gate Charge Test Circuit & Waveform

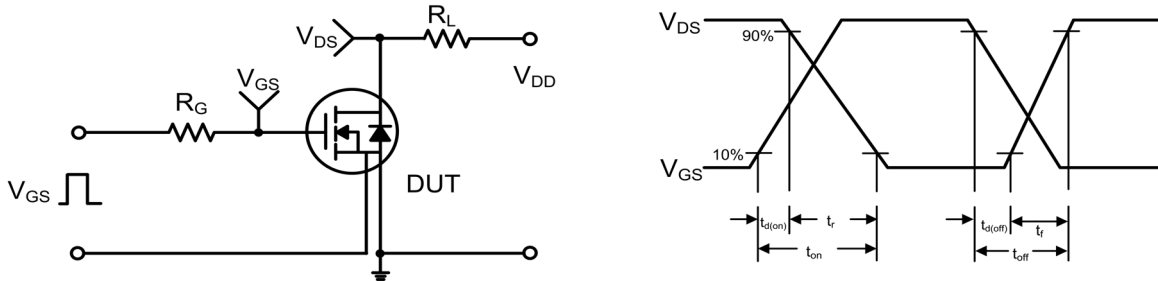


Figure 16. Resistive Switching Test Circuit & Waveforms

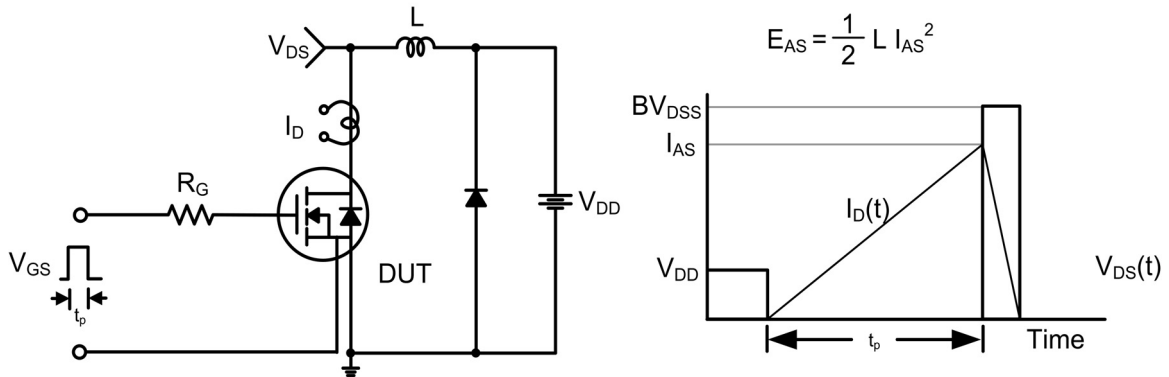


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

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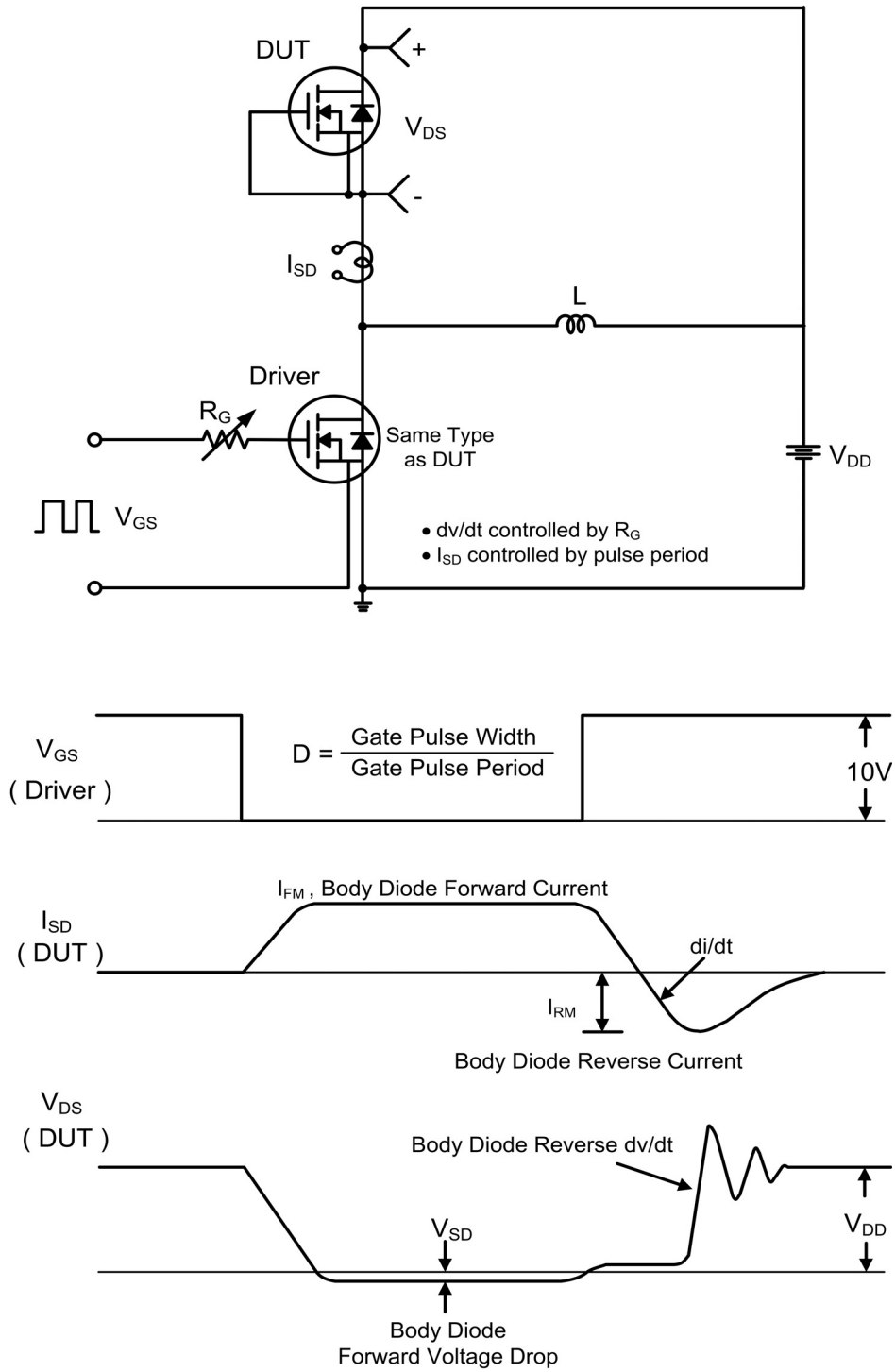


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

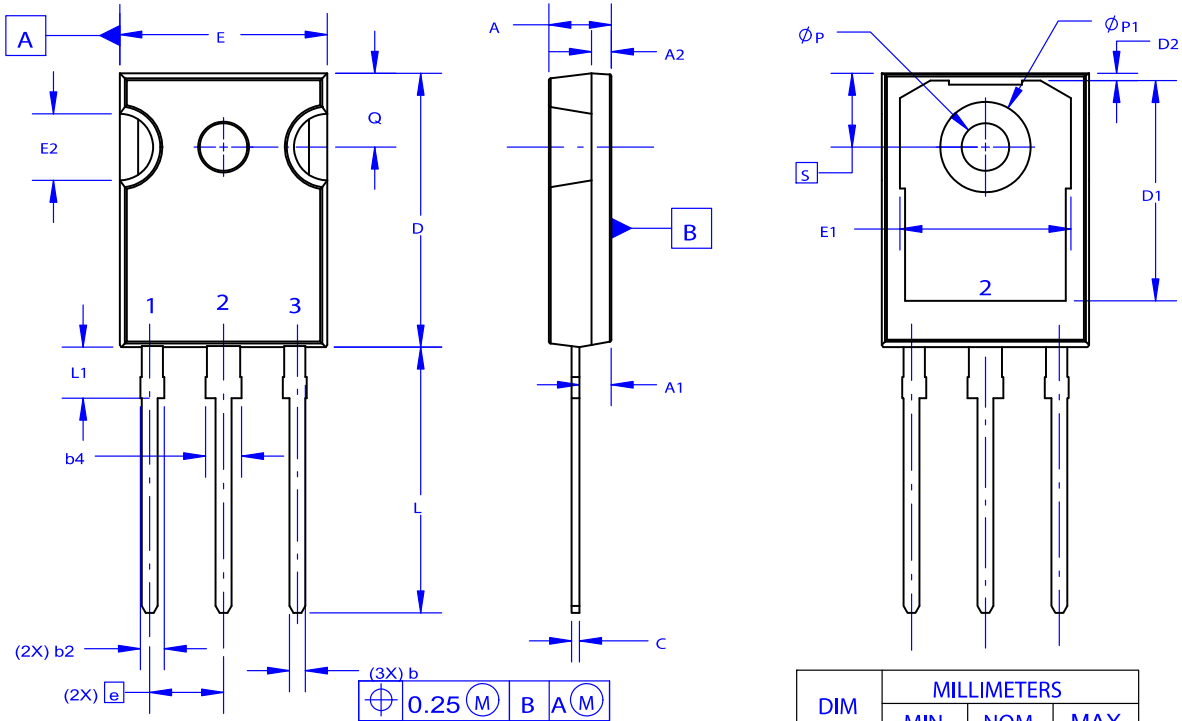
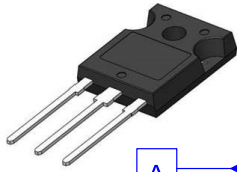
PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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